# FALL 2011
# ESE 501: System Specification and Modeling

Instructor: Prof. Sangjin Hong
Office: 217 Light Engineering Building
Office Hours: TueWed 1:30 p.m. - 3:30 p.m.
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## General Information

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| *Prerequisite:* | ESE 318 and ESE 330 or equivalent. Students are expected to know the logic design, digital circuits, and electronic design automation tools. Some background in computer architecture is helpful. |
| *Time and Place:* | TuTh 3:50p.m. - 5:10p.m. in Room 181 Earth & Space Building |
| *Teaching Assistants:* | No TA is available |
| *Textbook:* | System Design with SystemC by Grotket et al, Kluwer Academic Publishers, 2002. |
| *Reference:* | SystemC: Methodologies and Applications by W. Muller et al, Kluwer Academic Publishers, 2003. |
| *NOTE:* | |

## Course Goals

A comprehensive introduction to the field of System-on-Chip design. Introduces basic concepts of digital system modeling and simulation methodologies. Various types of hardware description language (HDL) will be studied, including Verilog, VHDL, and SystemC. Topics include top-down and bottom-up design methodology, specification language syntax and semantics, RTL, behavioral and system-level modeling, and IP core development. Included are three projects on hardware modeling and simulation.

## Project

This is a project-oriented course in which you will design three modest-sized systems. No specific lab times are scheduled, and you can work at your convenience.

## Course Contents

Week 1,2: Basics of RTL modeling in Verilog
Week 3,4: Basic behavioral modeling in SystemC
Week 5,6: Modeling Combinational Logic in SystemC
Week 7: Modeling Synchronous Logic in SystemC
Week 8: Miscellaneous Logic
Week 9,10,11: Digital system design using SystemC
Week 12: Design for testability
Week 13: IP cores design and integration

## Grading

The grade will be based upon:
(1) 3 Homeworks (30%)
(1) Projects (40%)
(3) 2 Exams (30%)

## Handouts

## Project Groups

Group 1: Names

## Announcements

*Last updated on:* 1 September, 2006